[FIELD EMISSION DISPLAY]

Abstract of Disclosure

A field emission display, having a cathode substrate with column lines thereon, a resistance layer covering the column lines, and gate rows crossing over the row lines. An insulation layer is located under the gate row lines to isolate the gate row lines. The resistance layer between the gate row lines is exposed. The insulation layer and the gate row lines have openings therein to expose the resistance layer. Micro-tips are formed on the exposed resistance layer in the openings. An anode substrate is located on the gate row lines and spaced with a vacuum space.